

REMARKS

Claims 1 - 9 are pending in the present application.

Applicants are amending claims 1, 3, 4, and 6 - 9 to correct punctuation, e.g., using semi-colons instead of commas, and to improve form, e.g., avoiding "adapted for" and "whereby". Applicants also amended claim 8 to clarify relationships between elements of the claim. None of the amendments is intended to narrow the scope of any term of any claim. Therefore, the doctrine of equivalents should be available for all of the terms of all of the claims.

On page 3 of the Office Action, claims 1 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,073,264 to Nelson et al. (hereinafter "the Nelson et al. patent") in view of U.S. Patent No. 6,055,285 to Alston (hereinafter "the Alston patent"). Applicants are traversing this rejection.

Claim 1 provides for a testing unit for testing a device under test (DUT). The testing unit includes a synchronizing unit that synchronizes a data flow of a response signal between the DUT and a receiving unit. The synchronizing unit receives a first clock signal from the DUT and a second clock signal from the testing unit, and includes (a) a buffer for buffering data, (b) a write unit for writing data from the DUT into the buffer, wherein the first clock signal controls a write access onto the buffer, and (c) a read unit for reading out data from the buffer to be provided to the receiving unit, wherein the second clock signal controls a read access onto the buffer.

The Nelson et al. patent discloses a system that includes a waveform acquisition unit (WAU) 40, a trigger unit (TU) 50 (see FIG. 1). WAU 40 receives test output from a DUT 60 (col. 2, lines 35 – 36). WAU 40 includes a DUT interface 440 (FIG. 4), that provides buffering for the DUT output signals (col. 4, lines 61 – 63). TU 50 outputs triggering signals to a trigger bus 52, by which the triggering signals are provided to WAU 40 and DUT 60 (FIG. 1). With reference to FIG. 5, the Nelson et al.

patent explains that TU 50 generates trigger signals that are synchronized to either a master clock from DUT 60 or a master triggering signal 34, as selected by a trigger multiplexer 525 (col. 5, lines 36 – 40).

The Office Action suggests that TU 50 is disclosure of a synchronizing unit, yet recognizes that the Nelson et al. patent does not disclose a synchronizing unit that includes a buffer, a write unit and a read unit. Thus, the Office Action introduces the Alston patent.

The Alston patent is directed toward a synchronization circuit for transferring data between two asynchronous circuits. As explained at col. 6, lines 10 – 16:

[A] transmitting circuit 102 operates in synchronism with a first clock signal (CLOCK1) on a first clock signal line 106, and the receiving circuit 104 operates in synchronism with a second clock signal (CLOCK2) on a second clock signal line 108. The two clock signals operate asynchronously with respect to each other and may have substantially different frequencies. (emphasis added).

Whereas in the Nelson et al. patent TU 50 generates trigger signals that are **synchronized** to either a master clock from DUT 60 or a master triggering signal 34, the system in the Nelson et al. patent has **no need for a synchronization circuit** for transferring data between two asynchronous circuits. Thus, there is no reason, and therefore **no motive**, to modify the system of the Nelson et al. patent to include the synchronizer of the Alston patent. Accordingly, the cited combination of the Nelson et al. and Alston patents is improper for purposes of a section 103(a) rejection of claim 1.

TU 50, as the Office Action recognizes, does not include a buffer for buffering data. Such is not surprising since TU 50 does not receive data from DUT 60. Additionally, as noted above, the Nelson et al. patent expressly states that DUT interface 440 provides buffering for the DUT output signals. If TU 50 were modified to include a buffer for buffering data, such a modification would apparently **obviate** the buffering operation of DUT interface 440, and **change the principle of operation** of the system disclosed by the Nelson et al. patent. Therefore, TU 50 of the Nelson et al. patent cannot be modified, by the Alston patent or any other reference, to include a buffer for purposes of a section 103(a) rejection of claim 1.

For the reasons provided above, Applicants submit that claim 1 is patentable over the cited combination of the Nelson et al. and Alston patents.

Claims 2 – 7 depend from claim 1. By virtue of this dependence, claims 2 – 7 are also patentable over the cited combination of references.

Claim 8 provides for a method of testing a DUT. The method includes (a) writing the data into a buffer, wherein the writing employs a first clock signal that controls a write access of the buffer, and wherein the first clock signal is provided by the DUT, and (b) reading the data from the buffer, wherein the reading employs a second clock signal that controls a read access of the buffer, and wherein the second clock is provided by a receiving unit.

The Office Action recognizes that the Nelson et al. patent does not disclose (a) writing data into a buffer, where a write access of the buffer is controlled by a first clock signal from a DUT, and (b) reading data from the buffer, where a read access of the buffer is controlled by a second clock signal from a receiving unit. Accordingly, the Office Action suggests that the Alston patent discloses an arrangement of two clocks and a buffer that can be used in combination with the system disclosed by the Nelson et al. patent.

However, as Applicants explained above during the discussion of claim 1, in the Nelson et al. patent, TU 50 generates trigger signals that are synchronized to either a master clock from DUT 60 or a master triggering signal 34, the system in the Nelson et al. patent has no need for a synchronization circuit for transferring data between two asynchronous circuits. Thus, there is no reason, and therefore no motive, to modify the system of the Nelson et al. patent to include the synchronizer of the Alston patent. Accordingly, the cited combination of the Nelson et al. and Alston patents is improper for purposes of a section 103(a) rejection of claim 8.

Additionally, as is also noted above, the Nelson et al. patent expressly states that DUT interface 440 provides buffering for the DUT output signals. If TU 50 were modified to include a buffer for buffering data, such a modification would apparently obviate the buffering operation of DUT interface 440, and change the principle of operation of the system disclosed by the Nelson et al. patent. Therefore, TU 50 of the Nelson et al. patent cannot be modified, by the Alston patent or any other reference, to include a buffer for purposes of a section 103(a) rejection of claim 8.

For the reasons provided above, Applicants submit that claim 8 is patentable over the cited combination of the Nelson et al. and Alston patents.

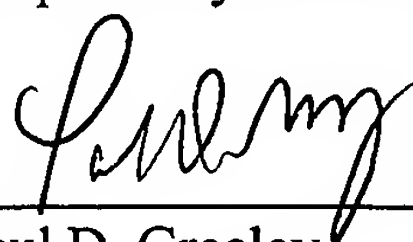
Claim 9 depends from claim 8. By virtue of this dependence, claim 9 is also patentable over the cited combination of references.

Applicants respectfully request reconsideration and withdrawal of the section 103(a) rejection of claims 1 – 9.

In view of the foregoing, Applicants respectfully submit that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicants respectfully request favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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